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(71) Applicant: APPLIED MATERIALS, INC. [US/US]; 3050 Bowers Avenue, Santa Clara, CA 95054 (US).

(72) Inventor: SOMEKH, Sasson; 25625 Moody Road, Los Altos Hills, CA 94022 (US).

(74) Agents: BERNADICOU, Michael, A. et al.; Blakely, Sokoloff, Taylor & Zafman LLP, 7th floor, 12400 Wilshire Boulevard, Los Angeles, CA 90025 (US).

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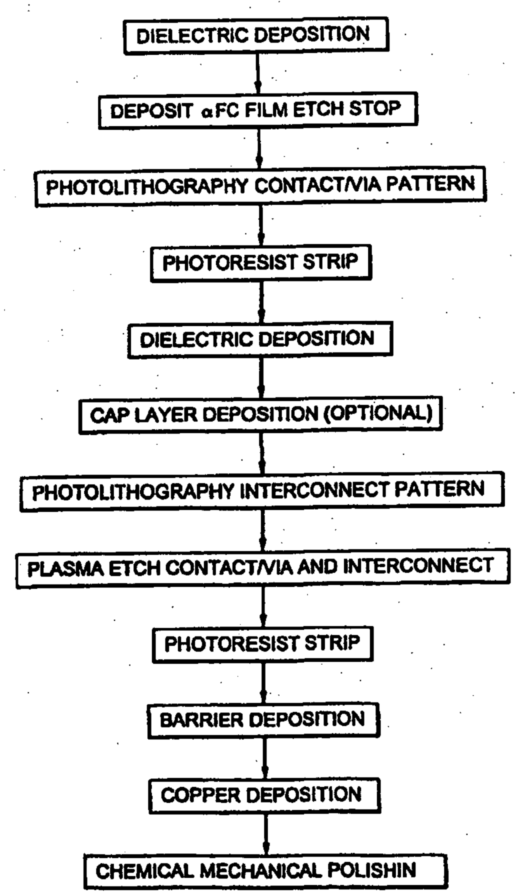
(54) Title: AN ETCH STOP LAYER FOR DUAL DAMASCENE PROCESS

(57) Abstract

The present invention provides a carbon based etch stop, such as a diamond like amorphous carbon, having a low dielectric constant and a method of forming a dual damascene structure. The low k etch stop is preferably deposited between two dielectric layers and patterned to define the underlying interlevel contacts/vias. The second or upper dielectric layer is formed over the etch stop and patterned to define the intralevel interconnects. The entire dual damascene structure is then etched in a single selective etch process which first etches the patterned interconnects, then etches the contacts/vias past the patterned etch stop. The etch stop has a low dielectric constant relative to a conventional SiN etch stop, which minimizes the capacitive coupling between adjacent interconnect lines. The dual damascene structure is then filled with a suitable conductive material such as aluminum or copper and planarized using chemical mechanical polishing.



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AN ETCH STOP LAYER FOR DUAL DAMASCENE PROCESS

BACKGROUND OF THE INVENTION

Field of the Invention

The present invention relates generally to the fabrication of integrated circuits on substrates. More particularly, the invention relates to a new etch stop layer and a process for forming a dual damascene structure characterized by a low capacitance between interconnect lines.

Background of the Invention

Consistent and fairly predictable improvement in integrated circuit design and fabrication has been observed in the last decade. One key to successful improvements is the multilevel interconnect technology which provides the conductive paths between the devices of an integrated circuit (IC) device. The shrinking dimensions of horizontal interconnects (typically referred to as lines) and vertical interconnects (typically referred to as contacts or vias: contacts extend to a device on the underlying substrate while vias extend to an underlying metal layer such as M1, M2, etc.) in very large scale integration (VLSI) and ultra large scale integration (ULSI) technology has increased the importance of reducing capacitive coupling between interconnect lines in particular. In order to further improve the speed of semiconductor devices on integrated circuits, it has become necessary to use conductive materials having low resistivity and low k (dielectric constant < 4.0) insulators to reduce the capacitive coupling between adjacent metal lines. For example, copper is now being considered as an interconnect material in place of aluminum because copper has a lower resistivity and higher current carrying capacity. Also, dielectric materials having a lower dielectric constant than that of silicon dioxide (dielectric constant ~4.0) are being seriously considered for use in production devices. One example of these dielectric materials is fluorine-doped silicon dioxide also known as fluorine-doped silicon glass (FSG) (dielectric constant ~3.5-3.7).

However, these materials present new problems for IC manufacturing processes. For example, because copper is difficult to etch in a precise pattern, traditional deposition/etch processes for forming interconnects has become unworkable, and accordingly, a process referred to as a dual damascene is being used to form copper interconnects. In a dual damascene process, the dielectric layer is etched to define both

the contacts/vias and the interconnect lines. Metal is then inlaid into the defined pattern and any excess metal is removed from the top of the structure in a planarization process, such as chemical mechanical polishing (CMP).

Figures 1a through 1c illustrate one method used in the fabrication of a dual damascene structure using a single (thick) dielectric layer 10 formed on a substrate 12. The dielectric layer 10 is patterned and etched using a timed etch process to define an interconnect line 20 as shown in Figure 1a. The vertical interconnects 16 (*i.e.*, contacts/vias), are then patterned in the bottom of the lines (Figure 1b) and etched to expose an underlying conductive or semiconductive layer such as a substrate 12 (Figure 1c). The etched structure having contacts/vias 16 and interconnects 20 is filled with a conductive material and the upper surface is planarized. However, the depth of the timed etch step is difficult to control and the patterning of the contacts/vias in the interconnect trenches is also a difficult process to perform.

Figures 2a and 2b illustrate another method used to fabricate a dual damascene structure. As shown in Figure 2a, a single (thick) dielectric layer 10 is formed on a substrate 12 and the contacts/vias 16 are patterned and partially etched through the dielectric layer 10 using a timed etch process. The interconnect lines 20 are then patterned and a second timed etch is conducted to form the trenches for the interconnects as shown in Figure 2b. During this second timed etch, the contacts/vias 16 are also etched to an additional depth sufficient for the contacts/vias to extend vertically to their intended depth as shown by the dashed lines. However, the timed etch steps again are difficult to control making this process less attractive for commercial production.

A third and more preferable method for fabricating a dual damascene structure uses a two-step dielectric deposition with an etch stop deposited therebetween as shown in Figure 3. A first dielectric layer 10 is deposited on a substrate and then an etch stop 14 is deposited on the first dielectric layer. The etch stop is then patterned to define the openings of the contacts/vias 16. A second dielectric layer 18 is then deposited over the patterned etch stop and then patterned to define the interconnect lines 20. A single etch process is then performed to define the interconnects down to the etch stop and to etch the unprotected dielectric exposed by the patterned etch stop to define the contacts/vias.

Silicon nitride has been the etch stop material of choice. However, the silicon nitride disposed between the dielectric layers is within the fringing field between the interconnects. Silicon nitride has a relatively high dielectric constant (dielectric constant

~7) compared to the surrounding dielectric, and it has been discovered that the silicon nitride may significantly increase the capacitive coupling between interconnect lines, even when an otherwise low k dielectric material is used as the primary insulator. This may lead to cross talk and/or resistance-capacitance (RC) delay which degrades the overall performance of the device.

Therefore, there is a need for a process to form a dual damascene with decreased capacitive coupling between interconnects.

Summary of the Invention

The present invention provides a process sequence and etch stop material which provides a reliable dual damascene structure while minimizing the contribution of the etch stop layer to the capacitive coupling between interconnect lines. In one embodiment, a low k dielectric film, such as an amorphous carbon (α-C) or amorphous fluorinated carbon (α-FC) film is used as the etch stop below an intermetal dielectric (IMD). Other low k materials such as parylene, AF_4, BCB, PAE, oxynitride and silicon carbide may also be used.

A preferred process sequence of the invention comprises depositing a first dielectric layer, such as a fluorinated silicate glass (FSG) layer, on a substrate, depositing a low k dielectric etch stop, such as an α-FC layer, on the first dielectric layer, patterning the etch stop to define the contacts/vias, depositing a second layer of a dielectric, such as FSG, patterning a resist layer on the second layer of dielectric to define one or more interconnects, and etching the interconnects and contacts/vias. The interconnects are etched down to the etch stop in the final etch step, and then the etching continues past the patterned etch stop to define the contacts/vias. Once the dual damascene structure has been formed, a barrier layer is preferably deposited conformably in the structure prior to filling the structure with copper to isolate the copper from other materials, such as silicon. The upper surface is then planarized using chemical mechanical polishing techniques.

Brief Description of the Drawings

So that the manner in which the above recited features, advantages and objects of the present invention are attained and can be understood in detail, a more particular

description of the invention, briefly summarized above, may be had by reference to the embodiments thereof which are illustrated in the appended drawings.

It is to be noted, however, that the appended drawings illustrate only typical embodiments of this invention and are therefore not to be considered limiting of its scope, for the invention may admit to other equally effective embodiments.

Figures 1a-1c are cross sectional views showing a prior art dual damascene process;

Figures 2a and 2b are cross sectional views showing a prior art dual damascene process;

Figure 3 is a cross sectional view showing a dual damascene structure formed on a substrate;

Figures 4a-4h are cross sectional views showing one embodiment of a deposition sequence of the present invention; and

Figure 5 is a process sequence for deposition of the dual damascene structure of Figure 4h.

<u>**Detailed Description of a Preferred Embodiment**</u>

The present invention provides an improved dual damascene structure comprising a low k etch stop, preferably an amorphous, diamond-like carbon (α-C) material. Low k etch stop is defined herein as an etch stop having a dielectric constant equal to or lower than that of silicon nitride (dielectric constant ~7.0). A dual damascene structure fabricated in accordance with the invention is shown in Figure 4h and the method of making the structure is sequentially depicted schematically in Figures 4a-4h, which are cross sectional views of a substrate having the steps of the invention formed thereon.

As shown in Figure 4a, an initial first dielectric layer 10, such as FSG, silicon oxide, or the like, is deposited on the substrate 12 to a thickness of about 5,000 to about 10,000 Å, depending on the size of the structure to be fabricated. As shown in Figure 4b, a low k etch stop 14, such as α-C, α-FC, parylene, AF_4, BCB, PAE, oxynitride or silicon carbide, is then deposited on the first dielectric layer to a thickness of about 200 to about 1000 Å. Low k etch stop 14 is then pattern etched to define the contact/via openings 16 and to expose first dielectric layer 10 in the areas where the contacts/vias are to be formed as shown in Figure 4c. Preferably, low k etch stop 14 is pattern etched

using conventional photolithography and etch processes using fluorine, carbon, and oxygen ions. After low k etch stop 14 has been etched to pattern the contacts/vias and the photoresist has been removed, a second dielectric layer 18 is deposited over etch stop 14 to a thickness of about 5,000 to about 10,000 Å as shown in Figure 4d. Second dielectric layer 18 is then patterned to define interconnect lines 20, preferably using conventional photolithography processes with a photoresist layer 22 as shown in Figure 4e. The interconnects and contacts/vias are then etched using reactive ion etching or other anisotropic etching techniques to define the metallization structure (*i.e.*, the interconnect and contact/via) as shown in Figure 4f. Any photoresist or other material used to pattern the etch stop 14 or the second dielectric layer 18 is removed using an oxygen strip or other suitable process.

The metallization structure is then formed with a conductive material such as aluminum, copper, tungsten or combinations thereof. Presently, the trend is to use copper to form the smaller features due to the low resistivity of copper (1.7 μΩ-cm compared to 3.1 μΩ-cm for aluminum). Preferably, as shown in Figure 4g, a barrier layer 24 such as tantalum, tantalum nitride, or other suitable barrier is first deposited conformally in the metallization pattern to prevent copper migration into the surrounding silicon and/or dielectric material. Thereafter, copper is deposited using either chemical vapor deposition, physical vapor deposition, electroplating, or combinations thereof to form the conductive structure. Once the structure has been filled with copper or other metal, the surface is planarized using chemical mechanical polishing, as shown in Figure 4h.

One embodiment of the invention contemplates the use of FSG as the intermetal dielectric, α-FC (dielectric constant ~2.8) as the etch stop and copper as the metal to complete the dual damascene structure. This process will now be described in detail below. The process steps for the following embodiment are shown in Figure 5.

A substrate is introduced into a DxZ® chamber available from Applied Materials, Inc., Santa Clara, California. A first blanket FSG layer of about 5000 Å is deposited on the substrate by flowing TEOS, O_2, and C_2F_6 or other gases over the substrate surface.

An oxide barrier layer may be deposited on the FSG layer to inhibit migration of species between the FSG layer and the subsequent α-FC layer.

Next, the substrate is moved to an Ultima^{tm} HDP-CVD chamber, also available from Applied Materials, Inc. of Santa Clara, California, where a 500 Å α-FC etch stop layer is formed on the first FSG layer. The α-FC etch stop layer is deposited by flowing octafluorocyclobutane (C_4F_8) and methane (CH_4) into the chamber at a rate of between about 20 sccm and about 200 sccm, preferably about 50 sccm. Argon, or other inert gas, is flown into the chamber at a rate of from about 20 sccm to about 100 sccm. A source power of 1000W and a bias power of 1000W are applied to the source coil and the substrate support member, respectively, to strike and maintain a high density plasma in the processing chamber. The chamber pressure during deposition is preferably less than 10 mTorr. While the above described process is preferred, other processes and precursor gases such as CH_4, C_2H_4, C_2H_6, C_2H_2, C_6H_6, CF_4, C_2F_6, C_3F_8, CHF_3, and C_6F_6 may also be used.

Next, a photoresist layer is formed over the α-FC etch stop layer and exposed by conventional photolithography methods to define the contact/via openings. The substrate is then moved to a dielectric etch chamber such as the IPS Chamber available from Applied Materials, Inc., of Santa Clara, California. The α-FC etch stop layer is preferably etched anisotropically with a high density plasma of trifluoromethane (CHF_3), O_2, and Ar to define the contact/via openings through the α-FC etch stop layer. Etching of the α-FC etch stop layer is preferably stopped prior to substantial etching of the underlying FSG layer to avoid over-etching. Endpoint detection between the α-FC film and the FSG layer is conveniently done by optical detection of the etch byproduct gases. The remaining photoresist layer is then stripped using an O_2 plasma.

The substrate is then moved back into the DxZ® chamber where a second 5,000 Å FSG layer is formed on the patterned α-FC etch stop layer. A second photoresist layer is then deposited on the second FSG layer and exposed by conventional photolithography methods to define the interconnect openings through the photoresist. The substrate is then returned to the IPS chamber and the entire dual damascene structure is etched in a single step by exposing the substrate to a carbon rich, oxygen free, fluorine-carbon etching environment. Preferably, the FSG layers are etched anisotropically with a plasma of C_3F_8 or C_3F_6 and Ar so that the interconnects and contacts/vias are formed with relatively straight sidewalls and no under cuts. Hydrogen can be added in small amounts to passivate the sidewalls. Once the interconnects are etched down to the patterned α-FC film, etching is substantially confined to the

patterned contacts/vias. Endpoint detection after etching through both FSG layers is conveniently done by optical detection of the etch byproduct gases. After etching of the interconnect is complete, the remaining resist layer is stripped using an O_2 plasma.

Preferably, a barrier layer of tantalum, tantalum nitride, combinations thereof, or other suitable barrier layer is formed over the patterned dual damascene structure and then the structure is filled with copper. One method which can be used to fill the structure with copper provides filling the contacts/vias with copper using CVD techniques and then filling the remaining volume of the structure using PVD techniques. However, any suitably filling process such as CVD, PVD (including high density plasma PVD), electroplating or combinations thereof may be used. The metal layer is then planarized by chemical mechanical polishing or other planarizing process prior to deposition of additional layers.

As shown in Figure 4h, a copper dual damascene structure is formed having a low k etch stop 14 disposed between the interconnects 26. The low k properties of the etch stop 14 prevent cross talk and increased RC delay between interconnects from adversely affecting the speed of the device.

Alternatives to α-C and α-FC etch stops include other carbon based materials. In particular, there are a number of carbon based materials that may be suitable etch stops for oxide intermetal dielectrics. Such materials which also have dielectric constants lower than SiN would reduce the capacitive coupling between interconnect lines. Such alternative carbon based films include parylene and related materials, such as parylene-N and AF_4, BCB spin-on, PAE, oxynitride and silicon carbide.

While the foregoing is directed to the preferred embodiment of the present invention, other and further embodiments of the invention may be devised without departing from the basic scope thereof, and the scope thereof is determined by the claims which follow.

Claims:

1. A method of forming a dual damascene structure, comprising:

depositing a first dielectric film on a substrate;

depositing a low k etch stop on the first dielectric film;

pattern etching the low k etch stop to define a vertical interconnect opening and expose the first dielectric film;

depositing a second dielectric film on the low k etch stop and the exposed first dielectric film; and

pattern etching the second dielectric film to define a horizontal interconnect and continuing to etch the exposed first dielectric film to define the vertical interconnect.

2. The method of claim 1 wherein the low k etch stop is selected from a group comprising α-FC, α-C, parylene, AF_4, BCB, PAE, oxynitride, silicon carbide and combinations thereof.

3. The method of claim 1 wherein the dielectric layer is comprised of fluorine doped silicon glass and the low k etch stop is comprised of α-FC.

4. The method of claim 3 further comprising depositing an oxide barrier layer before and after deposition of the low k etch stop.

5. The method of claim 1 wherein etching the horizontal and vertical interconnects is a single step etch process.

6. The method of claim 1 wherein the low k etch stop is α-FC.

7. The method of claim 6 wherein the α-FC etch stop is deposited from gases selected from the group comprising CH_4, C_2H_4, C_2H_6, C_2H_2, C_6H_6, CF_4, C_2F_6, C_3F_8, C_4F_8, CHF_3, and combinations thereof.

8. The method of claim 6 wherein the α-FC etch stop is deposited from gases comprising C_4F_8 and CH_4.

9. A method of forming a dual damascene structure, comprising:

depositing a first dielectric film on a substrate;

depositing a low k etch stop on the first dielectric film;

depositing a first photoresist layer on the low k dielectric etch stop;

patterning the first photoresist layer to define one or more vertical interconnect openings;

pattern etching the low k dielectric etch stop to define the one or more vertical interconnect openings and expose the first dielectric film;

stripping the first photoresist layer with an oxygen plasma;

depositing a second dielectric film on the low k dielectric etch stop and the exposed first dielectric film;

depositing a second photoresist layer on the second dielectric film;

patterning the second photoresist layer to define one or more horizontal interconnects;

pattern etching the second dielectric film to define the one or more horizontal interconnects and continuing to etch the first dielectric film to define the one or more vertical interconnects.

10. The method of claim 9 wherein the low k etch stop is selected from a group comprising α-FC, α-C, parylene, AF_4, BCB, PAE, oxynitride, silicon carbide and combinations thereof.

11. The method of claim 9 wherein the dielectric layer is comprised of fluorine doped silicon glass and the low k etch stop is comprised of α-FC.

12. The method of claim 11 further comprising depositing an oxide barrier layer before and after deposition of the low k etch stop.

13. The method of claim 9 wherein etching the horizontal and vertical interconnects is a single step etch process.

14. The method of claim 9 wherein the low k etch stop is α-FC.

15. The method of claim 14 wherein the α-FC etch stop is deposited from gases selected from the group comprising CH_4, C_2H_4, C_2H_6, C_2H_2, C_6H_6, CF_4, C_2F_6, C_3F_8, C_4F_8, CHF_3, and combinations thereof.

16. The method of claim 14 wherein the α-FC etch stop is deposited from gases comprising C_4F_8 and CH_4.

17. A dual damascene structure, comprising:

a) a first low k dielectric layer defining one or more vertical interconnects;

b) a low k patterned etch stop overlying the first low k dielectric layer and patterned to define the one or more vertical interconnects;

c) a second low k dielectric layer overlying the patterned low k etch stop and defining one or more horizontal interconnects; and

d) wherein the low k patterned etch stop layer comprises a material having a dielectric constant at least equal to or lower than that of the first or second dielectric layer.

18. The structure of claim 17 wherein the low k etch stop comprises amorphous carbon.

19. The structure of claim 18 wherein the first and second dielectric layers are comprised of a material selected from fluorine doped silicon oxide, silicon oxide or combinations thereof.

20. The structure of claim 17 wherein the low k etch stop comprises a material selected from α-FC, α-C, parylene, AF_4, BCB, PAE, oxynitride, silicon carbide and combinations thereof.

21. The structure of claim 19 wherein the one or more vertical interconnects and the one or more horizontal interconnects are comprised of a metal selected from aluminum, copper, tungsten or combinations thereof.

22. The structure of claim 21 further comprising a barrier layer disposed between the low k dielectrics and the metal.

23. The structure of claim 22 wherein the barrier layer is comprised of tantalum, tantalum nitride, titanium, titanium nitride, silicon nitride or combinations thereof.

24. An etch stop comprised of a carbon based material having a dielectric constant less than 7.

25. The etch stop of claim 24 wherein the carbon based material is selected from the group comprising α-FC, α-C, parylene, AF_4, BCB, PAE, oxynitride, silicon carbide and combinations thereof.

26. A carbon based film having a dielectric constant less than SiN used as an etch stop below a silicon based intermetal dielectric.

27. A carbon based film having a dielectric constant less than SiN used as an etch stop below a silicon based intermetal dielectric in a dual damascene structure.

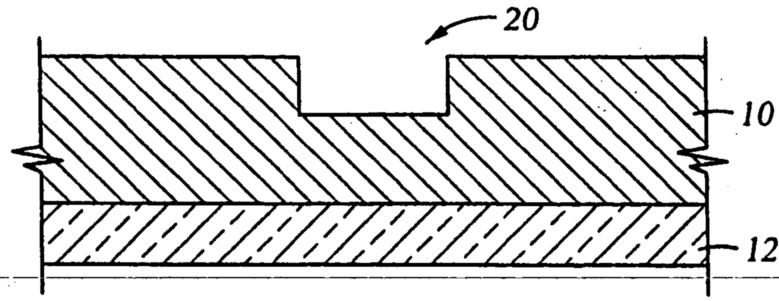


Fig. 1a
(PRIOR ART)

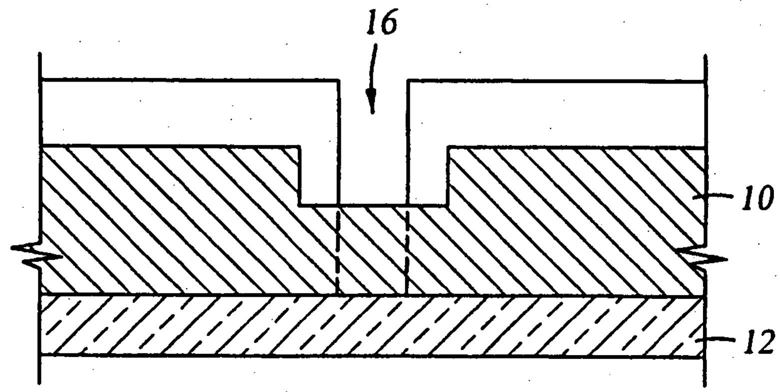


Fig. 1b
(PRIOR ART)

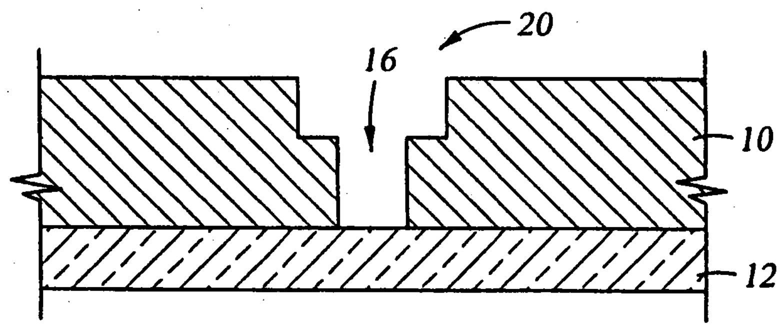


Fig. 1c
(PRIOR ART)

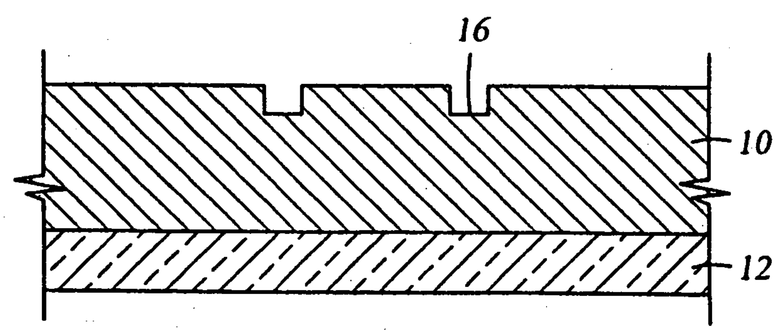


Fig. 2a
(PRIOR ART)

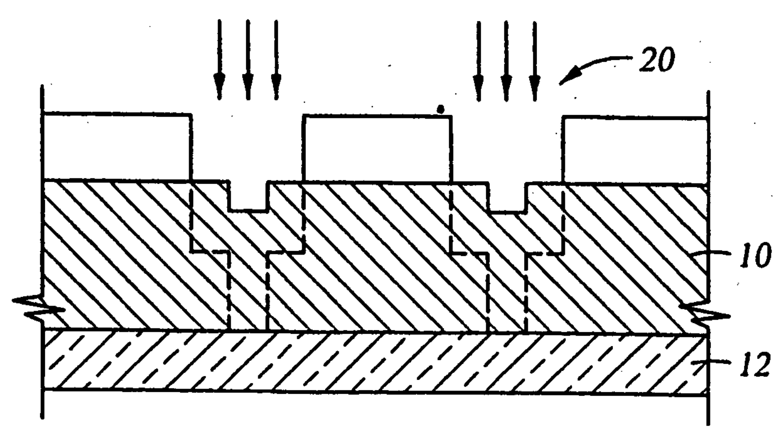


Fig. 2b
(PRIOR ART)

Fig. 3

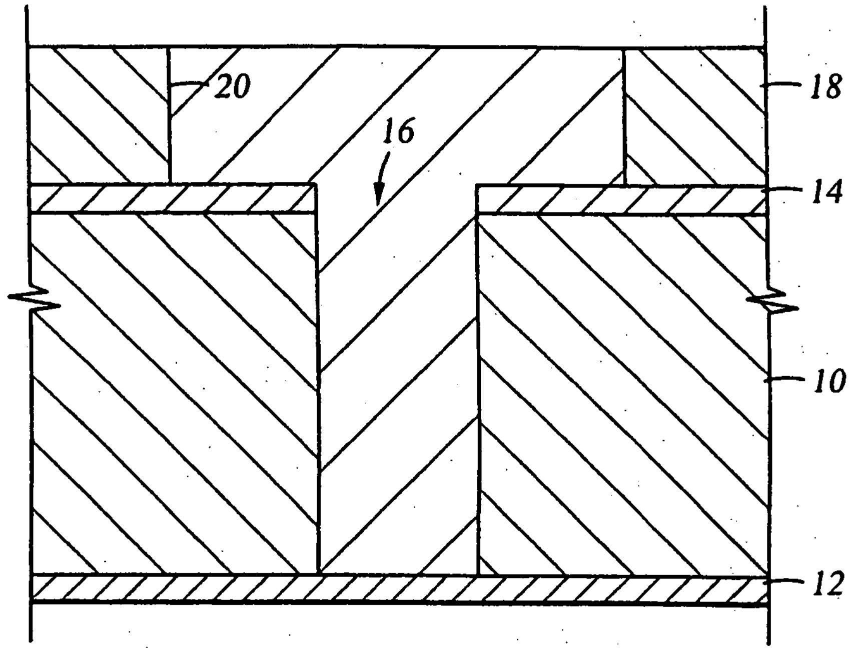


Fig. 4a

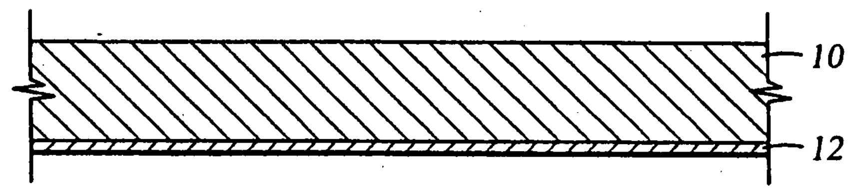


Fig. 4b

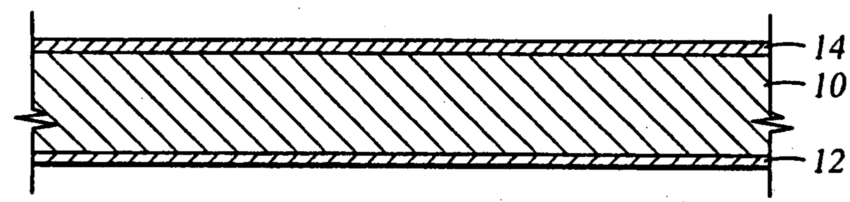


Fig. 4c

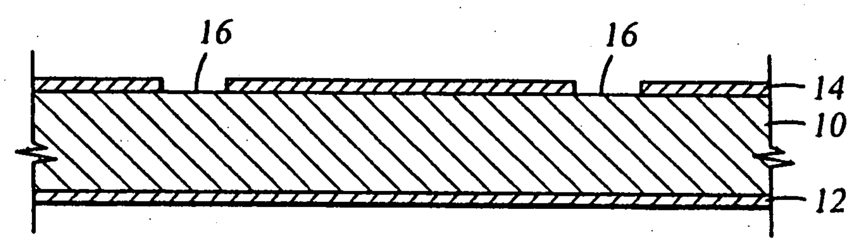


Fig. 4d

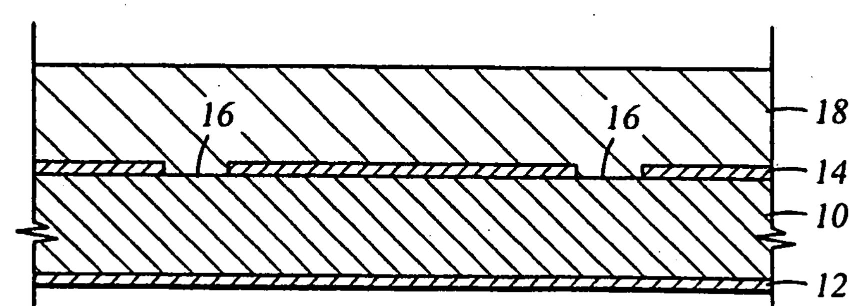


Fig. 4e

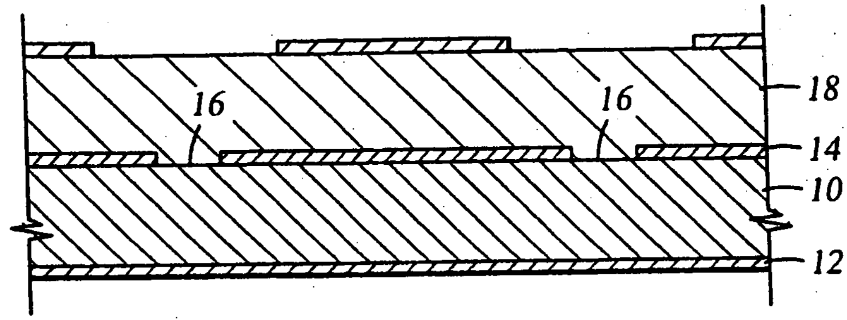


Fig. 4f

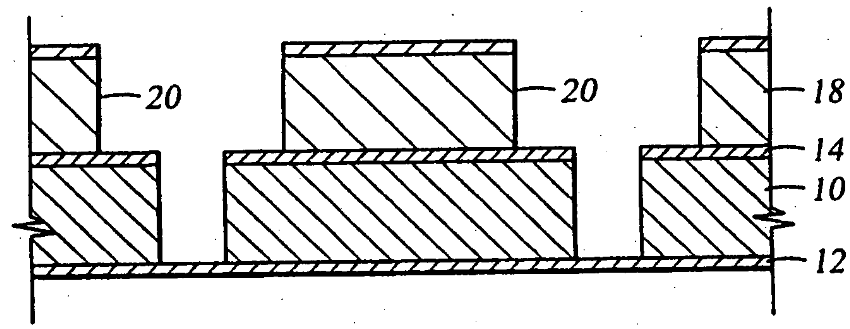


Fig. 4g

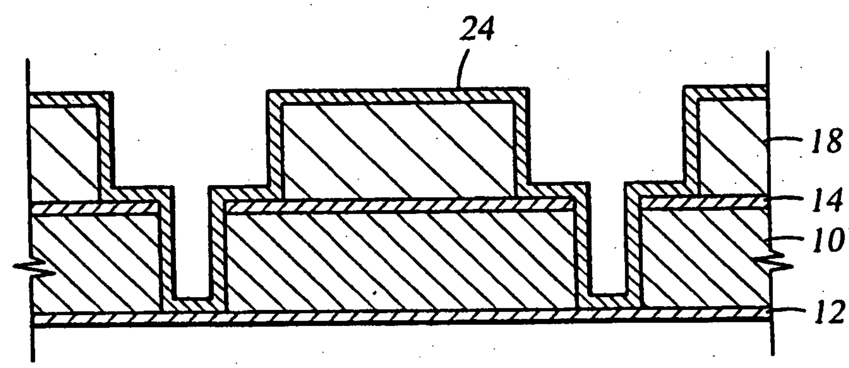
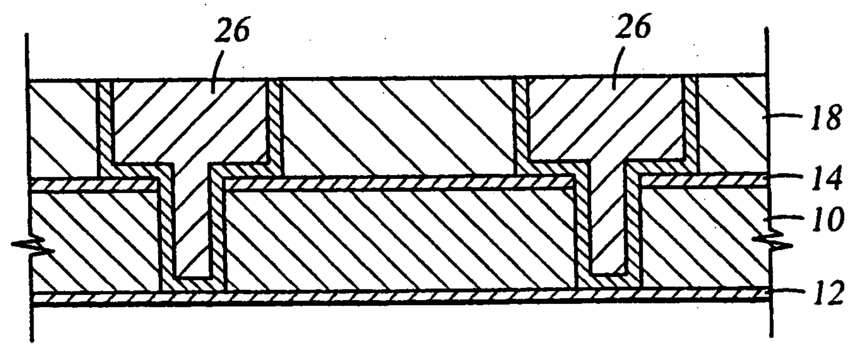
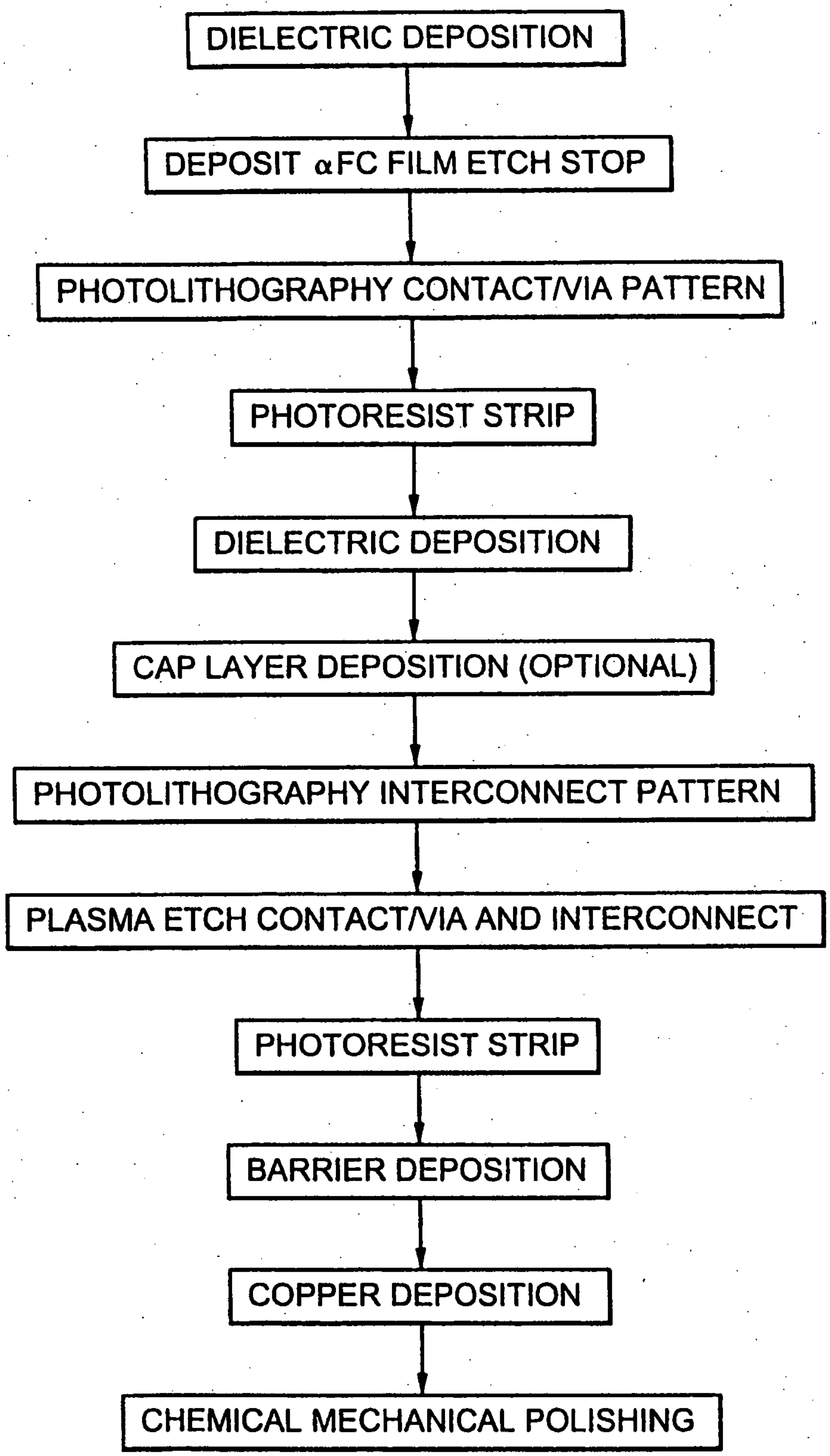


Fig. 4h

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DEPOSIT αFC FILM ETCH STOP
PHOTOLITHOGRAPHY CONTACT/VIA PATTERN
PHOTORESIST STRIP
DIELECTRIC DEPOSITION
CAP LAYER DEPOSITION (OPTIONAL)
PHOTOLITHOGRAPHY INTERCONNECT PATTERN
PLASMA ETCH CONTACT/VIA AND INTERCONNECT
PHOTORESIST STRIP
BARRIER DEPOSITION
COPPER DEPOSITION
CHEMICAL MECHANICAL POLISHING

Fig. 5

INTERNATIONAL SEARCH REPORT

International Application No
PCT/US 98/23888

A. CLASSIFICATION OF SUBJECT MATTER
IPC 6 H01L21/768

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 6 H01L C23C

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	EP 0 224 013 A (IBM) 3 June 1987 see column 4, line 1 - column 5, line 11 ---	1,2,5,6,9,10,13,14,17-21,27
Y	EP 0 696 819 A (IBM) 14 February 1996 see column 3, line 56 - column 4, line 57 see column 9, line 52 - column 11, line 17	1,2,5,6,9,10,13,14,17-21,27
X		24-26
A	---	22,23

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[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

° Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

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Date of the actual completion of the international search	Date of mailing of the international search report
24 February 1999	03/03/1999
Name and mailing address of the ISA European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Authorized officer Schuermans, N

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INTERNATIONAL SEARCH REPORT

Intı .ional Application No
PCT/US 98/23888

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

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A	"DAMASCENE: OPTIMIZED ETCH STOP STRUCTURE AND METHOD" IBM TECHNICAL DISCLOSURE BULLETIN, vol. 36, no. 11, 1 November 1993, page 649 XP000424980 ---	
A	EP 0 768 388 A (NIPPON ELECTRIC CO) 16 April 1997 see column 5, line 50 - line 57 see column 7, line 10 - line 17 see column 8, line 55 - column 9, line 29 see claim 9 -----	7,8,15, 16

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INTERNATIONAL SEARCH REPORT

Information on patent family members

International Application No
PCT/US 98/23888

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